Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size = .0023 x .0029”**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 9/23/21**

**MFG: SILICON SUPPLIES THICKNESS .007” P/N: BFT93W**

**DG 10.1.2**

#### Rev B, 7/1